There is a little work on the specifics of managing Field Programmable Gate Array (FPGA) resources, specifically memory units, in a secure manner. This paper concentrates on two important approaches which are proposed by Huffmire et al. These approaches are
1) Usage of a reconfigurable reference monitor, which enforces the legal sharing of memory among cores.
2) Usage of moats and drawbridges which exploits the spatial nature of computation on FPGAs to provide strong isolation of the cores. To understand the practical issues of these protection primitives, especially the first one, for FPGAs, the researchers are working on to build an embedded system consisting of multiple cores on a single FPGA. FPGAs and their security issues provide an attractive research area. This paper is in this research area which makes the paper very interesting and its future work very promising. The approach, which starts with simple architecture and moves to the complex architecture and additional units, is very good. Having the writer of the referenced papers gives significant advantage to improve the future policies and design improvements. So, the problem, solution for the problem, and the approach for solving the problem is agreeable.

Major Comments:
1) It is best to give a little more information about the goal of the paper in the introduction section. Instead of using one sentence to summarize, you need to add another sentence to describe multiple cores or just to name them.
2) Your approach to the solution is right, so stating the approach that you used, and using the results of every step will make the paper more understandable and significant.
3) In the related work section, “Reconfigurable Protection” and “Covert Channels, Direct Channels, and Trap Doors” subsections are related to the related work section. However, there is no relation between intellectual property (IP) theft and your paper. If you think that there is a relation, state it more comprehensible. If there is no relation and this subsection is just for additional information, you need to give more information to make it coherent.
4) Place Figure 1 to a place which is in the same page with the subsection “Reconfigurable Protection”. This figure is described in this subsection.
5) The system architecture is explained very well in the project proposal. However, in this paper, there is not enough information about the system architecture. It is best to use the writing in the project proposal.
6) Like 5, there must be more information in the progress and future work subsections of the system architecture section.
7) You stated that you modified the serial code to work with the new file format. Give more information about this modification.
8) Section 3.2, reference monitor with the OPB block ram controller was the first step of the implementation and you stated that it functions correctly with low latency and overhead. Please quantify these results.
9) Give more information about the policy of the system and combine this information with the DFA which enforces this policy.
10) Moving Communication Interface section after the System architecture section will make the paper more coherent.

Minor Comments:
1) Give the long form of TLB, DFA.
2) There is some unrelated information in the caption of Figure 1 like the goal of the paper. Make it concise.
3) Don’t construct sentences like “Of course the techniques..” or “We believe..”
4) Figure 2 and Figure 3 is not explained the paper. Captions need to be more concise.

Generally, you didn’t give enough information for your system architecture, policy and communication interface. And you didn’t quantify the results of the system architecture in intermediate steps. Adding these will make your paper flawless. It can be seen that you had very significant progress in the project, and the future work can be completed till the end of this quarter. However, there is not enough time to incorporate the TDMA arbiter and secure DMA controller into the bus architecture (This part is taken from the proposal). After completing the project excluding the arbiter and DMA controller, I recommend you to use your project in conjunction with Chien and Byuns work to see that how promising this is.